

**PATENT**  
**(5681-67300/P9675)**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 10/696,891  
Filed: October 30, 2003  
Inventor(s):  
Robert E. Cypher

§ Examiner: Unknown  
§ Group/Art Unit: 2131  
§ Atty. Dkt. No: 5681-67300  
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Title: **ECC FOR COMPONENT  
FAILURES USING  
GALOIS FIELDS**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel

Name of Registered Representative

  
Signature

April 9, 2004

Date

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☒ the additional information identified below in paragraph 3.

- ☒ A copy of each required reference listed on the Form PTO-1449 is enclosed.
- ☐ The references listed on the Form PTO-1449 were previously cited in application serial no. \_\_\_\_\_ to which the captioned application is seeking priority under 35 U.S.C. § 120; therefore, a copy of each reference is not enclosed.
- ☒ The present application is a U.S. national patent application filed after June 30, 2003, or an international application that entered the national stage under 35 USC § 371 after June 30, 2003. Therefore, copies of the cited U.S. patents and/or U.S. patent application publications are not enclosed.

1. This Information Disclosure Statement is submitted:

- a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);

- ☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
- ☒ before the mailing date of a first Office Action on the merits; or
- ☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.
- b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of \$180.00 is enclosed.
- c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of \$180.00 is enclosed.

2. It is hereby certified:

- ☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in § 1.56(c) more than thirty (30) days prior to the filing of the information disclosure statement;
- ☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of the Statement; or
- ☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three (3) months prior to the filing of the Statement.
3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

U.S. Application Serial No. 10/637,469	(5681-67200)
U.S. Application Serial No. 10/185,265	(5181-96700)
U.S. Application Serial No. 10/184,674	(5181-96800)
U.S. Application Serial No. 10/185,959	(5681-32200)

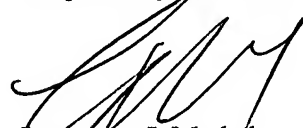
4. For each non-English language reference listed on the attached Form PTO-1449:

- ☐ reference is made to an English language translation submitted herewith, and/or
- ☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or
- ☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

- ☐ reference is made to the concise explanation contained in the specification of the present application at page(s) \_\_\_\_\_, and/or
- ☐ reference is made to the concise explanation set forth below:
5. ☐ Applicant also offers the following comments for the Examiner's consideration:
6. ☐ Also enclosed is a copy of a foreign search report citing these references.
7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.
8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzl, P.C. Deposit Account No. 501505/5681-67300/LJM.

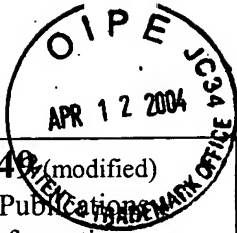
Respectfully submitted,



Lawrence J. Merkel  
Reg. No. 41,191  
Attorney for Applicant(s)

MEYERTONS, HOOD, KIVLIN,  
KOWERT & GOETZEL, P.C.  
P. O. Box 398  
Austin, Texas 78767  
(512) 853-8800

Date: April 9, 2004

**Form PTO-1449** (modified)List of Patents and Publications  
For Applicant's Information  
Disclosure Statement  
(Use several sheets if necessary)

ATTY. DKT. NO. 5681-67300

APPLICANT: Robert E. Cypher

FILING DATE: October 30, 2003

SERIAL NO. 10/696,891

GROUP: 2131

**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
		6,473,880	10/29/02	Cypher			
		6,453,440	9/17/02	Cypher			
		6,393,597	5/21/02	Cypher			
		6,477,682	11/5/02	Cypher			
		6,367,046	4/2/02	Chapman, et al.			
		6,301,780	10/16/01	Templeton			
		5,574,856	11/12/96	Morgan, et al.			
		5,251,219	10/5/93	Babb			
		4,617,664	10/14/86	Aichelmann, Jr., et al.			
		6,141,789	10/31/00	Cypher			
		6,282,686	8/28/01	Cypher			
		6,233,716	5/15/01	Cypher			
		6,301,680	10/9/01	Cypher			

**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

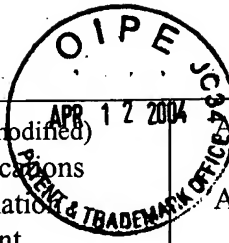
**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

	A1	Dell Computer Corp., David Locklear, "Chipkill Correct Memory Architecture," August 3, 2000, 3 pages.
	A2	Dell, "A White Paper on the Benefits of Chipkill-Correct ECC for PC Server Main Memory," IBM Microelectronics Division, November 1997, pp. 1-23.
	A3	"The IBM Eserver pSeries 690, Reliability, Availability, Serviceability (RAS)," IBM Technical White Paper, Sept. 2001, 24 pages.
	A4	"Parallel Parity," <a href="http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/block.htm">http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/block.htm</a> , 1994, 1 pg.
	A5	"Modulo-2 Arithmetic," <a href="http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/modulo.htm">http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/modulo.htm</a> , 1994, 1 pg.
	A6	"Introduction to Error Control," <a href="http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/intro.htm">http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/intro.htm</a> , 1994, 1 pg.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

**Form PTO-1449** (modified)

List of Patents and Publications

For Applicant's Information

Disclosure Statement

(Use several sheets if necessary)

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APPLICANT: Robert E. Cypher

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**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

	A7	Barker et al. "ASCII Table," <a href="http://www.eng2.uconn.edu/cse/Cour...08W/References/Ref_ASCIITable.html">http://www.eng2.uconn.edu/cse/Cour...08W/References/Ref_ASCIITable.html</a> , February 1998, 1 pg.
	A8	"Parity & Computing parity," <a href="http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/parity.htm">http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/parity.htm</a> , 1994, 2 pgs.
	A9	"Error Correction with Hamming Codes," <a href="http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/hamming.htm">http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/hamming.htm</a> , 1994, 2 pgs.
	A10	Barker et al. "Hamming Code, Background Information," <a href="http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Background.html">http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Background.html</a> , February 1998, 3 pgs.
	A11	Barker et al., "Hamming Code, Theory," <a href="http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Theory.html">http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Theory.html</a> , March 1998, 2 pgs.
	A12	"NUMA: Delivering the Next Level of Commodity SMP Performance," <a href="http://199.245.235.23/newsletters/html/vpoint5.html">http://199.245.235.23/newsletters/html/vpoint5.html</a> , 1996, 4 pgs.
	A13	Barker et al. "General Definitions," <a href="http://www.eng2.uconn.edu/cse/Cour...8W/References/Ref_Definitions.html">http://www.eng2.uconn.edu/cse/Cour...8W/References/Ref_Definitions.html</a> , February 1998, 3 pgs.
	A14	Barker et al. "Hamming Code, Lab Procedure," <a href="http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Procedure.html">http://www.eng2.uconn.edu/cse/Courses/CSE208W/Hamming/Procedure.html</a> , June 1998, 3 pgs.
	A15	Burskirk, "32-Bit-Wide Memory Tolerates Failures," NT Tech Notes, October 1990, p. 818.
	A16	C. L. Chen, "Symbol Error Correcting Codes for Memory Applications," IBM Corporation, IEEE, 1996, pages 200-207.
	A17	IEEE Transactions of Computers, Vol. 41, No. 2, February 1992, 5 pages.
	A18	Hamada, et al., "A Class of Error Control Codes for Byte Organized Memory Systems -SbEC-(Sb+S)ED Codes-," IEEE Transactions of Computers, Vol. 46, No. 1, January 1997, 5 pages.
	A19	Costello, Jr., et al., "Applications of Error-Control Coding," IEEE Transactions on Information Theory, Vol. 44, NO. 6, October 1998, pages 2531-2560.
	A20	Ziegler, et al., "Cosmic Ray Soft Error Rates of 16-Mb DRAM Memory Chips," IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998, pages 246-252.
	A21	Peterson, et al., "Error-Correcting Codes," Second Edition, The MIT Press, 1972, pages 357-373.
	A22	Shu Lin, "Error Control Coding, Fundamental and Applications," Prentice-Hall, 1983, pp. 503-525 and 532.

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Information Disclosure Statement--PTO 1449 (modified)